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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,749	06/12/2001	Andrew M. Draper	015114-053600US	5820

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	6

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/880,749	Applicant(s) DRAPER, ANDREW M.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because this application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Claim Objections

Claim 3 is objected to because on line 2, before the word "allows", the term "is" must be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-26, 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: The structural limitation for a "***programmable logic portion***" recited in claims 1, 11, 21 and 28 lacks a structural cooperative relationship with the proceeding limitations for "a first and a second JTAG circuit".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Jones (US 5768288), ISSUED: June 16, 1998.

Regarding independent Claims 1, 11, 21, 27, Jones discloses a method and apparatus for programming and testing integrated circuits, comprising:

A programmable logic portion, in FIG. 5 which illustrates prior art test logic 500 which operates in accordance with the JTAG specification, where the test logic 500 is coupled to memory 528 comprising memory locations in a programmable logic device under test configuration (FIG. 4b) illustrating multiple devices under test 430 and 446 coupled with each other through their respective test circuits 434 and 450.

A first JTAG test circuit 434, which is shown in detailed as test logic 500, FIG. 5, comprising a TAP controller 503 coupled to a first instruction register 506 including a d plurality of data registers (508, 512, 514).

A second JTAG test circuit 450, which is the identical mirror of test circuit 434, and which is shown in detailed as test logic 500, FIG. 5, comprising a TAP controller 503 coupled to a second instruction register 506 including a plurality of data registers (508, 512, 514), where the first JTAG test circuit 434 is coupled to the second JTAG

test circuit 450, FIG. 4b. The test logic 500, which is similar to the test circuit in the device under test (2408, FIG. 24), communicates with digital signal processing device 2402.

Regarding Claims 2, 3, 12, 13, 22 and 23, Jones discloses a data register (508) for loading data into the programmable logic portion (432, 448) and for transmitting and receiving data from the programmable logic portion.

Regarding Claim 4, 14 and 24, data register, such as boundary scan register (512) for communicating through MUX 516 between the embedded logic portion of the integrated circuit and the external host processor, using digital signal processing device (2402, FIG. 24).

Regarding Claims 5-8, 15-18 and 28, Jones discloses an external host processor such as digital signal processing device 2402 having a memory 2404 comprising a computer system, a microprocessor, or any other device capable of reading the set of instructions stored on medium 2402, executing the set of instructions and providing the appropriate clock, mode select and data signals to the device under test 2408 via interconnect 2406.

Regarding Claims 9, 10, 19, 20, 25, 26 and 29, Jones discloses second plurality of data registers (508, 512, 514) of the second JTAG test circuit 450, FIG. 4b, which are coupled to a first multiplexer (516) FIG. 5, controlled by data signal (526) decoded from (504) and an output of the multiplexer (516), instruction register (506) with the test data output (TDO) connected to (TDI) input from the first JTAG test circuit (450, FIG. 4b) are coupled to a second multiplexer controlled by the TAP controller (503).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James C Kerveros
Examiner
Art Unit 2133

By: _____

Guy J. Lamare
for
Albert DeCady
Primary Examiner

U.S. PATENT OFFICE
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Date: 3/3/04
Office Action : Non-Final Rejection